Doc. Number:

☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: N156BGN
SUFFIX: E41

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
1.0	Apr.14, 2015	All	Spec Ver.1.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N156BGN-E41 is a 15.6“ diagonal TFT Liquid Crystal Display module with LED Backlight unit and 40 pins eDP interface. This module supports 1366 x 768 HD mode and can display 262,144 colors. The optimum viewing angle is at 6 o’clock direction

1.2 GENERAL SPECIFICATI0NS

LCD TFT Module + TP Module Combination			
Item	Specification	Unit	Note
Luminance, White	200	Cd/m2	
Surface Hardness	3H, Glare	-	
Color Gamma	45%	NTSC	
Thickness	3.20 max(W/O PCB), 3.40 max. (With PCB)	mm	
LCD TFT Module			
Item	Specification	Unit	Note
Driver Element	a-si TFT active matrix	-	
Pixel Arrangement	RGB vertical stripe	-	
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.252 (H) x 0.252 (V)	mm	
Display Colors	262,144	color	-
Interface	eDP 1.2	-	
Transmissive Mode	Normally white		
Power Consumption	Total (3.41) W (Max.)@cell (0.72) W (Max.), BL (2.69) W (Max.)	-	(1)
TP Module			
Item	Specification	Unit	Note
Number of Channels	40 x 70	-	
Touch Method	Finger	-	
Numbers of Touch	10 points	-	
Accuracy	Meet WHCK	mm	
Linearity	Meet WHCK	-	
Reporting rate	>100Hz	Hz	
Interface	USB 2.0	-	
Link Power Management	L1	-	
Power Consumption	Active mode (0.32)W , Idle mode(0.16)W	-	(2)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas Mosaic pattern is displayed.

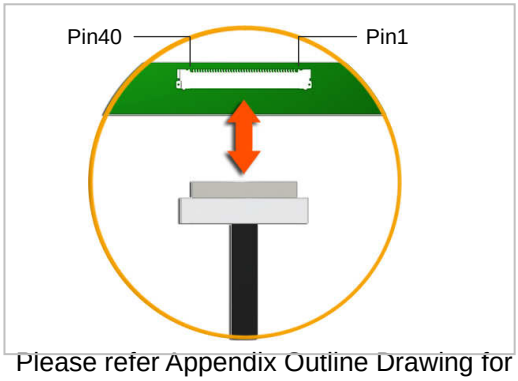
Note (2) The active mode is under the conditions at report rate 100Hz and 5 fingers touch

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	359	359.5	360	mm	(1)
	Vertical (V)	206	206.5	207	mm	
	Thickness (T)	-	3.05	3.2	mm	
Bezel Area	Horizontal	--	347.83	--	mm	
	Vertical	--	196.94	--	mm	
Active Area	Horizontal	344.13	344.23	344.33	mm	
	Vertical	193.44	193.54	193.64	mm	
Glass Thickness	CF	0.35	0.4	0.45	mm	
	TFT	0.35	0.4	0.45	mm	
Weight		-	325	345	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12 or equivalent

User's connector Part No: IPEX-20453-040T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS of ENVIRONMENT

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

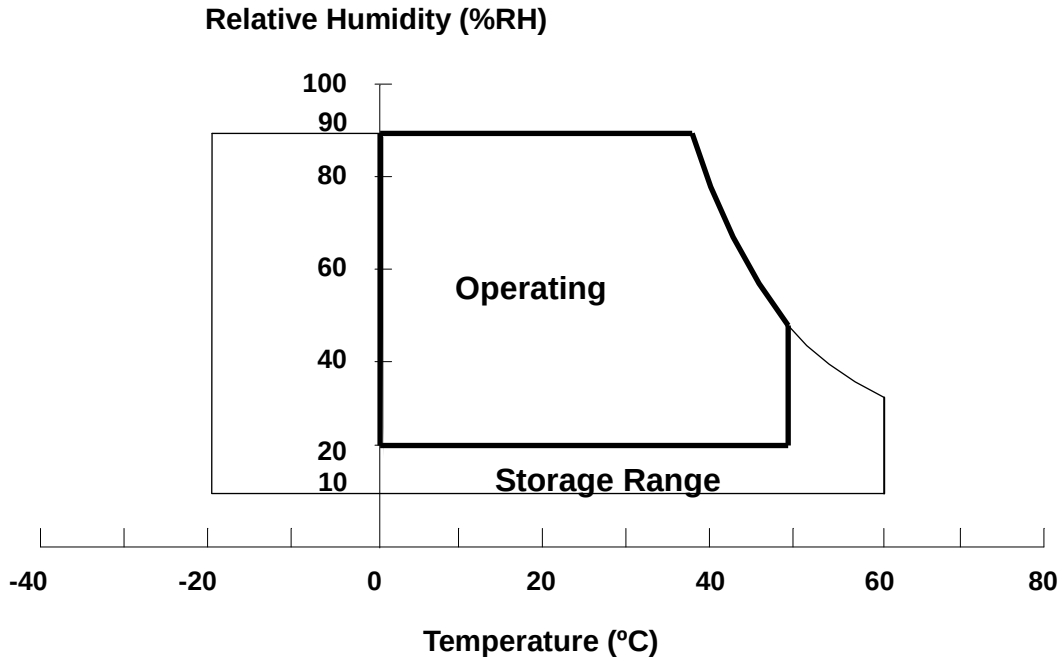
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



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4. OPTICAL CHARACTERISTICS

4.1 TEST CONDITIONS

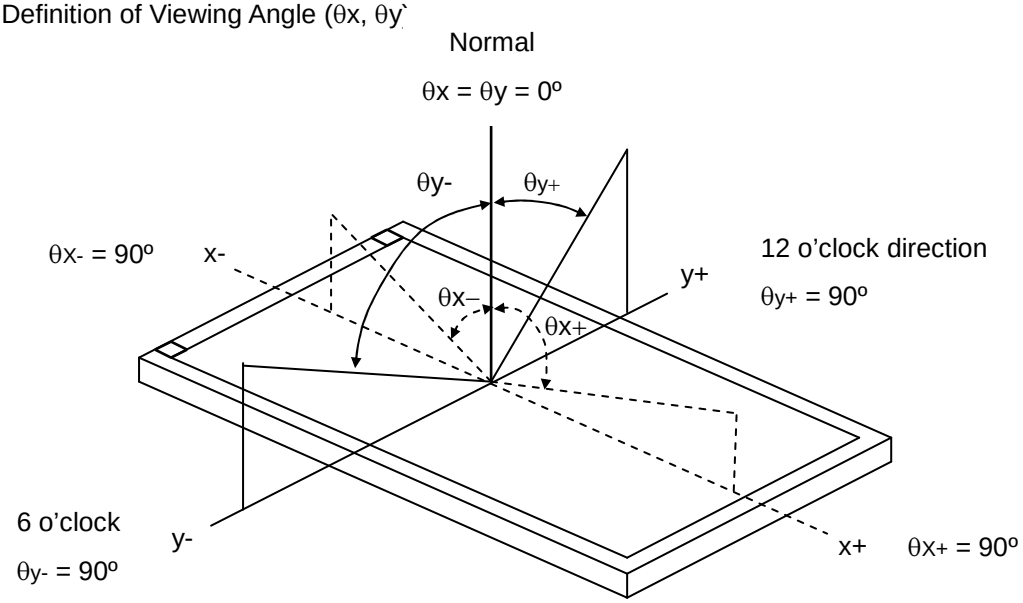
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	120	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

4.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	400	600	-	-	(2), (5) (7)
Response Time		T_R		-	3	8	ms	(3), (7)
		T_F		-	7	12	ms	
Average Luminance of White		L_{AVE}		170	200	-	cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	(0.572)	Typ + 0.03	-	(1),(7)
		Ry			(0.336)		-	
	Green	Gx			(0.324)		-	
		Gy			(0.584)		-	
	Blue	Bx			(0.160)		-	
		By			(0.141)		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45		Deg.	(1),(5), (7)
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80	-	-	%	(5),(6), (7)

Note (1) Definition of Viewing Angle (θx, θy`



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

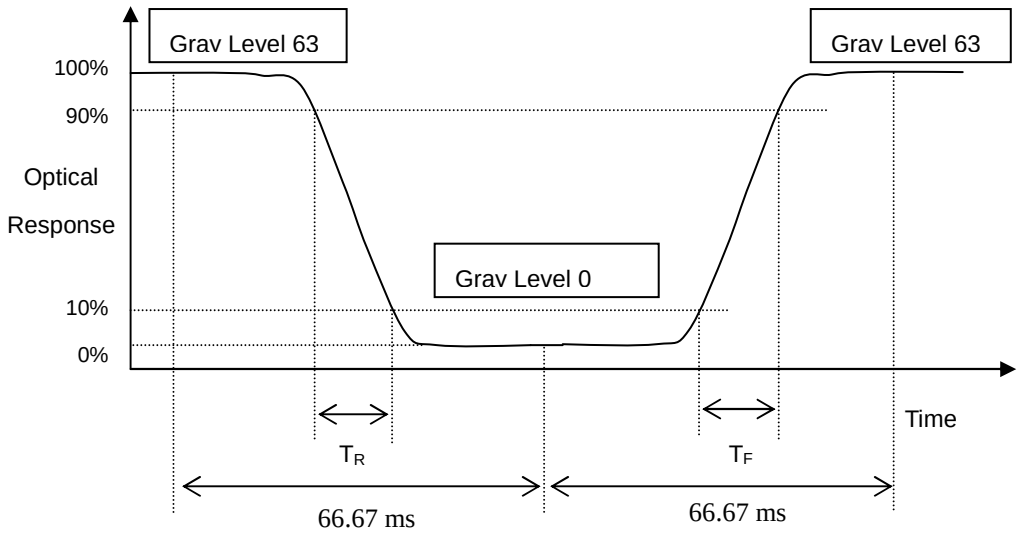
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

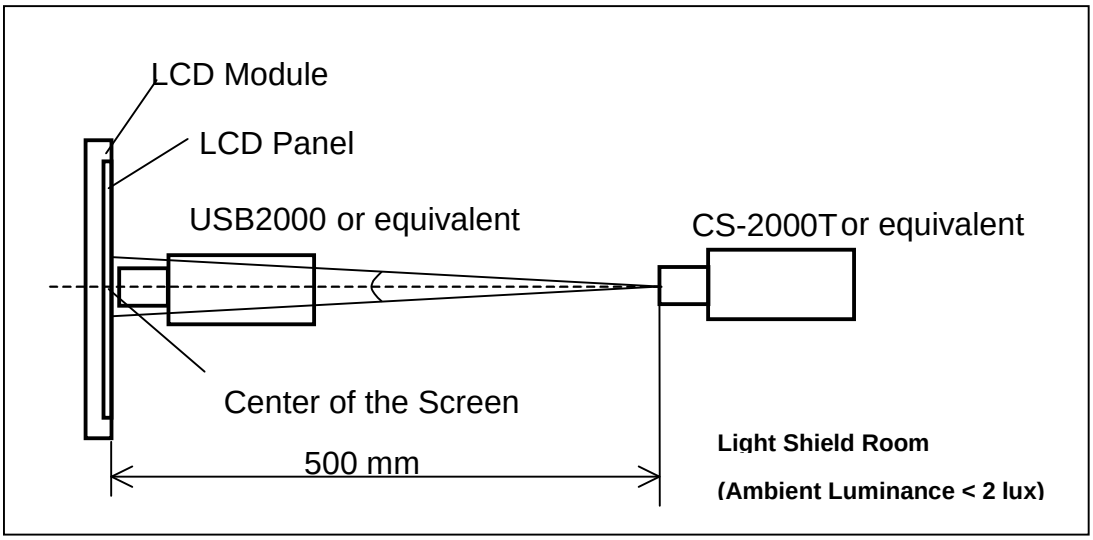
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

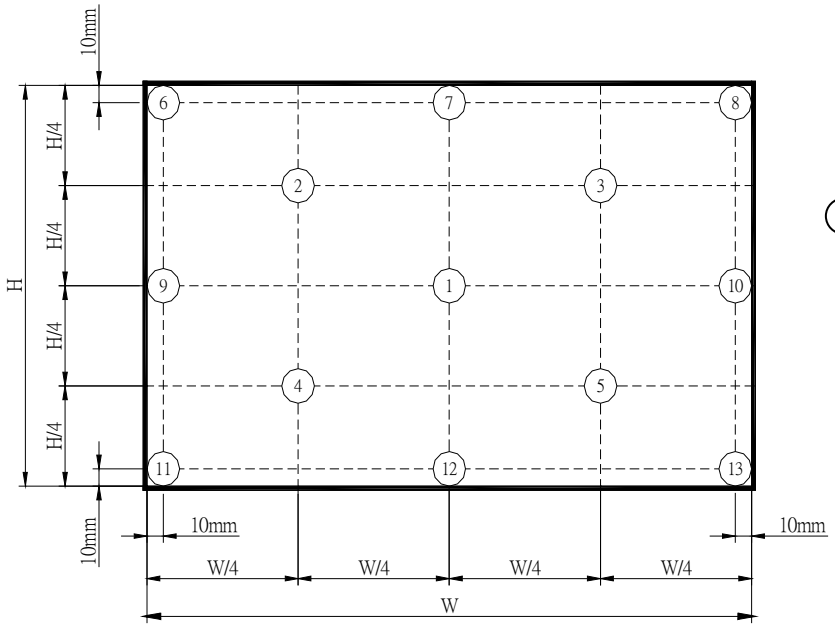


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Minimum [L (1)~ L (5)] / Maximum [L (1)~ L (5)]}*100%

δW_{13p} = {Minimum [L (1)~ L (13)] / Maximum [L (1)~ L (13)]}*100%



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

5. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

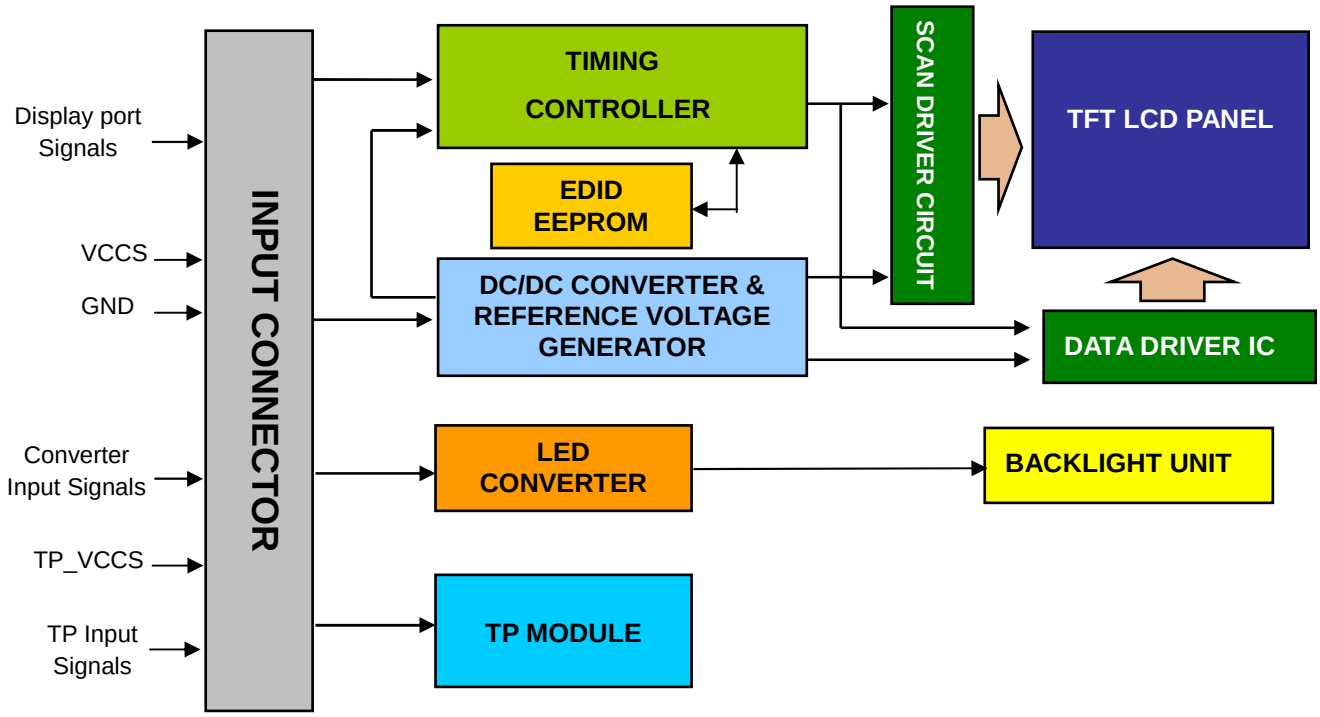
Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture

6. ELECTRICAL SPECIFICATIONS

6.1 FUNCTION BLOCK DIAGRAM



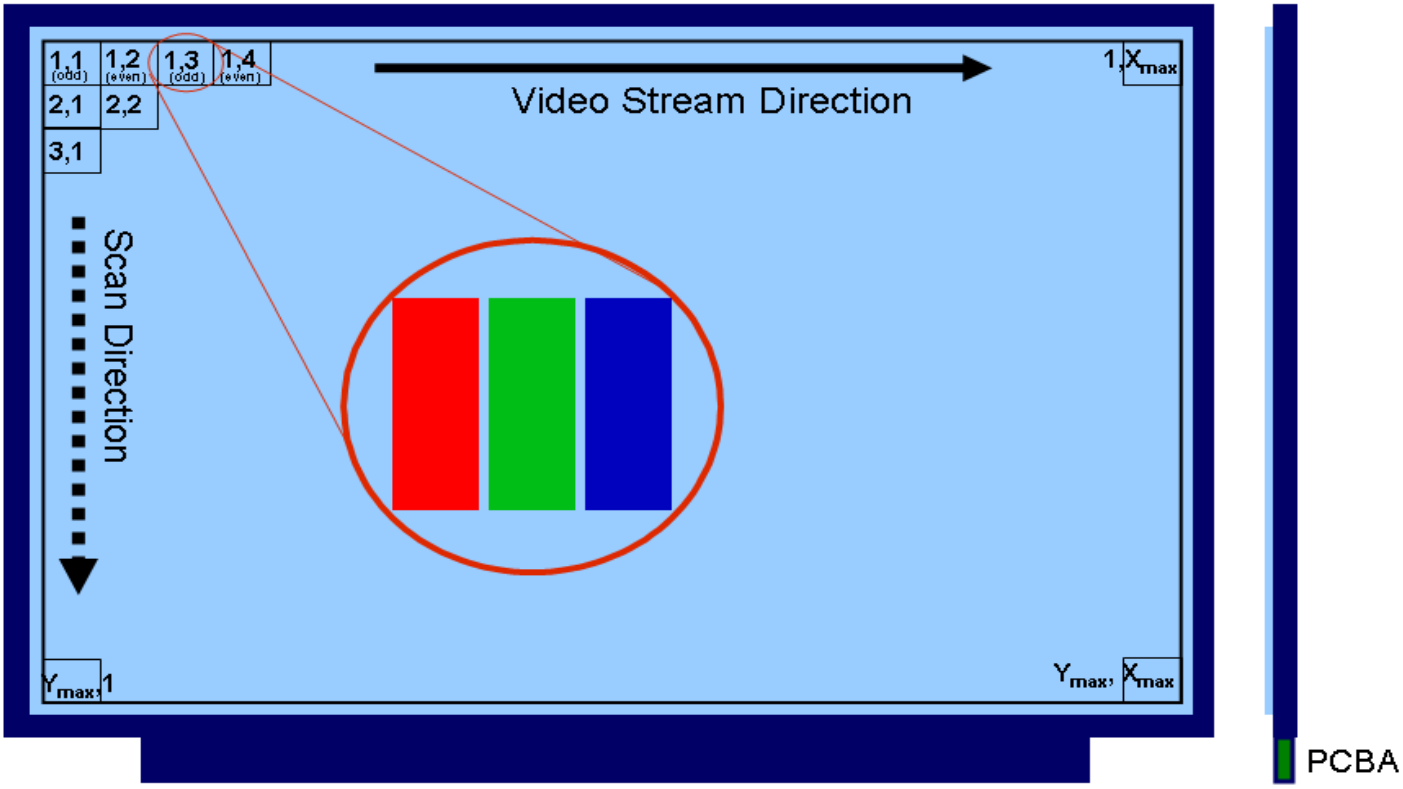
6.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserve)	
2	H_GND	High Speed Ground	
3	NC	No Connection (Reserve for Lane1_N)	
4	NC	No Connection (Reserve for Lane1_P)	
5	H_GND	High Speed Ground	
6	Lane0_N	Complement Signal-Lane 0	
7	Lane0_P	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	Aux_Ch_P	True Signal-Auxiliary Channel	
10	Aux_Ch_N	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply for LCD	
13	VCCS	Power Supply for LCD	
14	NC	No Connection (Reserve)	
15	VSS	Ground	
16	VSS	Ground	
17	HPD	Hot Plug Detect	
18	LED_GND	LED Ground	
19	LED_GND	LED Ground	
20	LED_GND	LED Ground	

21	LED_GND	LED Ground	
22	LED_EN	Enable Control Signal of LED Converter	
23	LED_PWM	PWM Control Signal of LED Converter	
24	NC	No Connection (Reserve)	
25	NC	No Connection (Reserve)	
26	LED_VCCS	LED Power Supply	
27	LED_VCCS	LED Power Supply	
28	LED_VCCS	LED Power Supply	
29	LED_VCCS	LED Power Supply	
30	NC	No Connection (Reserve)	
31	TP_USB-	USB Data- for Touch panel	
32	TP_USB+	USB Data+ for Touch panel	
33	TP_VSS	USB Ground for Touch panel	
34	TP_VCCS	Power Supply for Touch panel(5V)	
35	TP_VCCS	Power Supply for Touch panel(5V)	
36	TP_RS	Touch panel report switch(High : Enable, Low : Disable)	
37	NC	No Connection (Reserve)	
38	NC	No Connection (Reserve)	
39	NC	No Connection (Reserve)	
40	TP_Reset	Reset signal for Touch panel(High : Normal, Low :Reset)	

Note (1) The first pixel is odd as shown in the following figure.



7. LCD ELECTRICAL CHARACTERISTICS

7.1.1 LCD ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	(26)	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	(5)	V	1)
Converter Control Signal Voltage	LED_EN	-0.3	(5)	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “LCD ELETRONICS SPECIFICATION”

7.1.2 LCD ELETRONICS SPECIFICATION

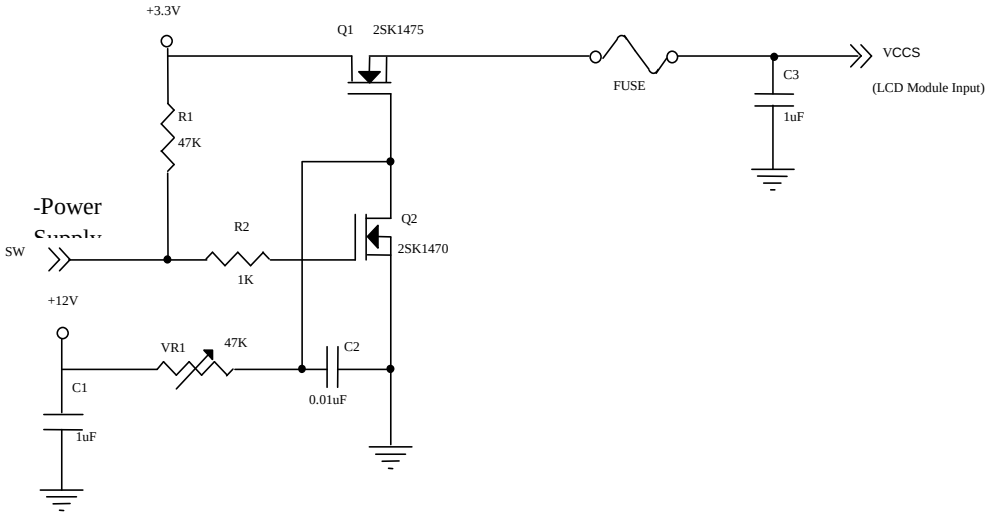
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		V_{RP}	-	50	-	mV	(1)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc		(180)	(217)	mA	(3)a
	Black			(180)	(217)	mA	(3)
HPD Impedance		R_{HPD}	30K			ohm	(4)
HPD	High Level		2.25	-	2.75	V	(5)
	Low Level		0	-	0.4	V	(5)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

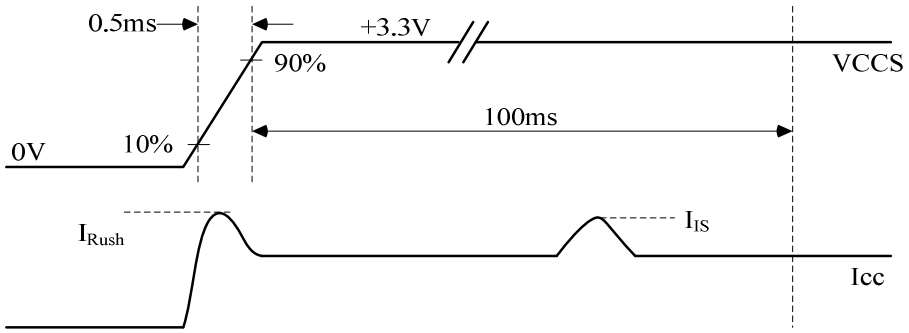
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

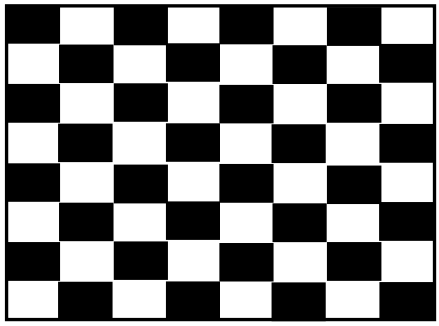


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (5) When a source detects a low-going HPD pulse longer than 2ms in duration, it must be regarded as a hot-plug-event HPD pulse. Upon detecting this hot-plug-event HPD pulse, the source must read the receiver capability field and link / sink status field of the DPCD and take corrective action

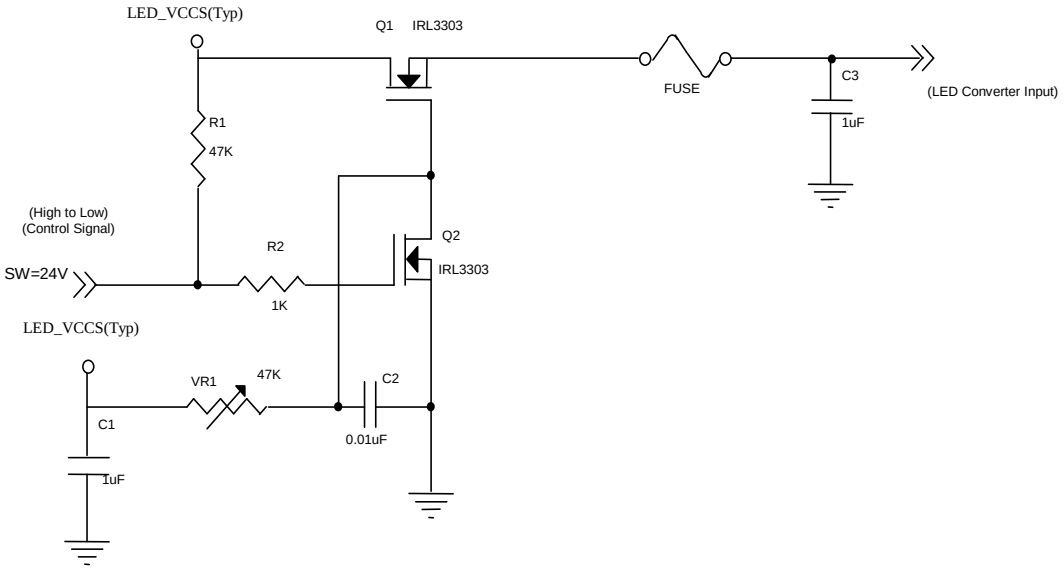
7.1.3 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_Vccs	(5.0)	(12.0)	(21.0)	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On		(2.2)	-	(5.0)	V	(4)
	Backlight Off		0	-	(0.6)	V	(4)
LED_EN Impedance		R_{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level		(2.2)	-	5	V	(4)
	PWM Low Level		0	-	(0.6)	V	(4)
PWM Impedance		R_{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio			(5)	-	100	%	(5)
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	
PWM Control Frequency		f_{PWM}	(190)	-	(2K)	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED	(166)	(209)	(224)	mA	(3)

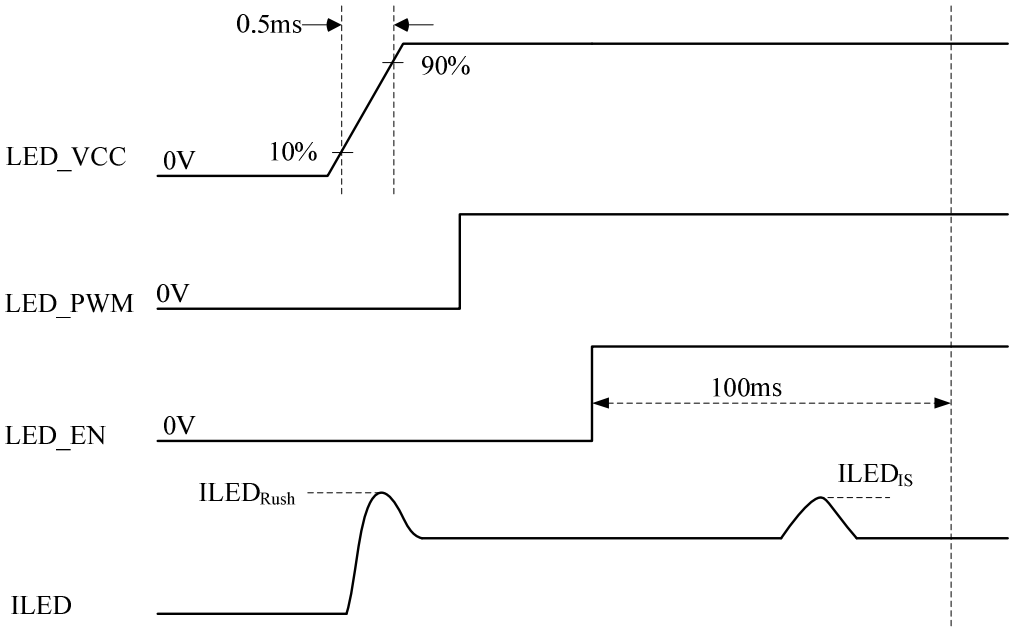
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

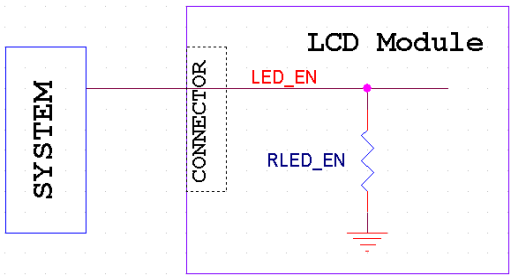
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



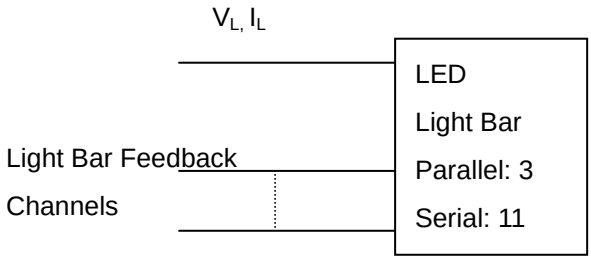
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

7.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	(28.6)	31.9	(33)	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	64.5	-	mA	
Power Consumption	P_L	-	2.058	(2.129)	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 oC and IL = 21.5 mA(Per EA) until the brightness becomes ≦ 50% of its original value

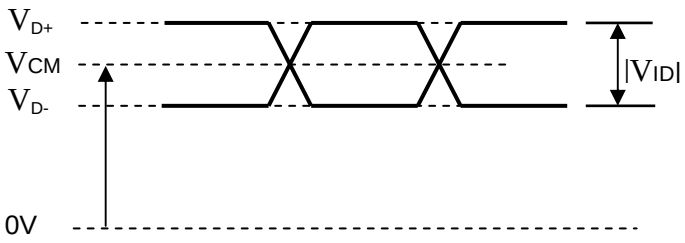
7.3 DISPLAY PORT SIGNAL TIMING SPECIFICATION

7.3.1 DISPLAY PORT INTERFACE

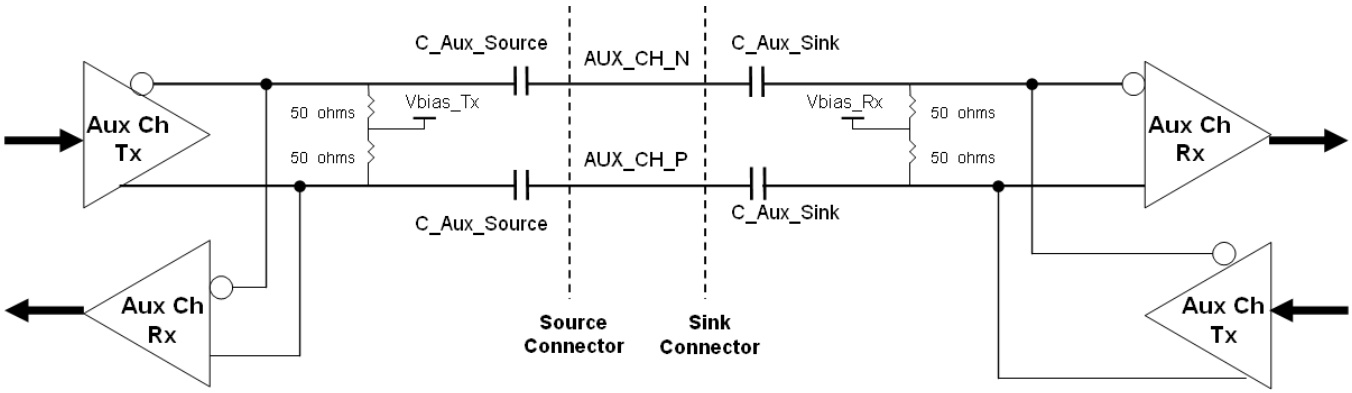
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

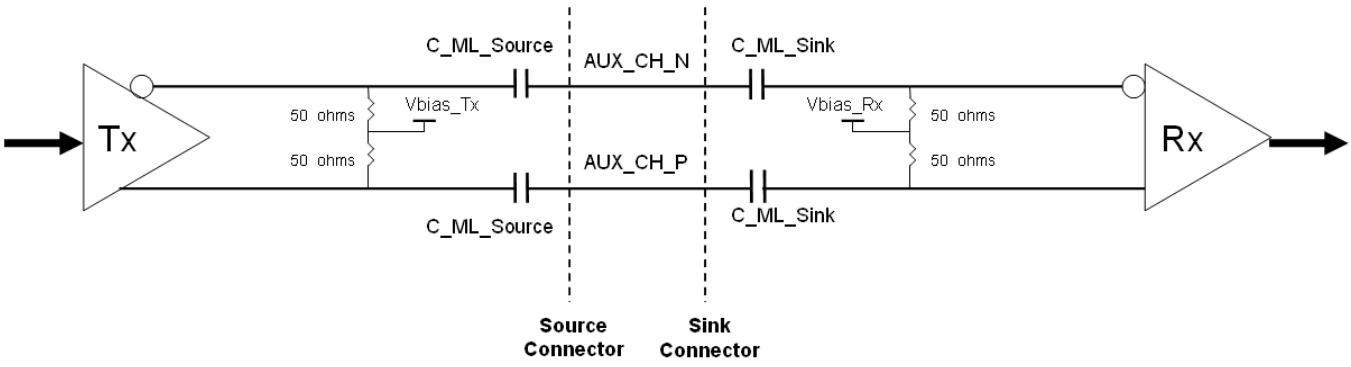
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

7.3.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

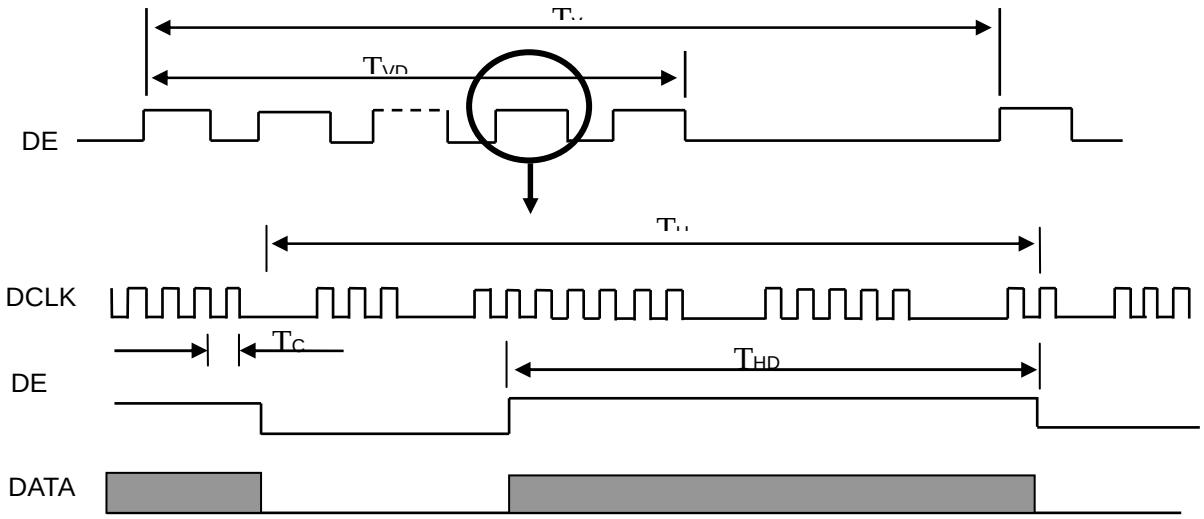
7.4 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

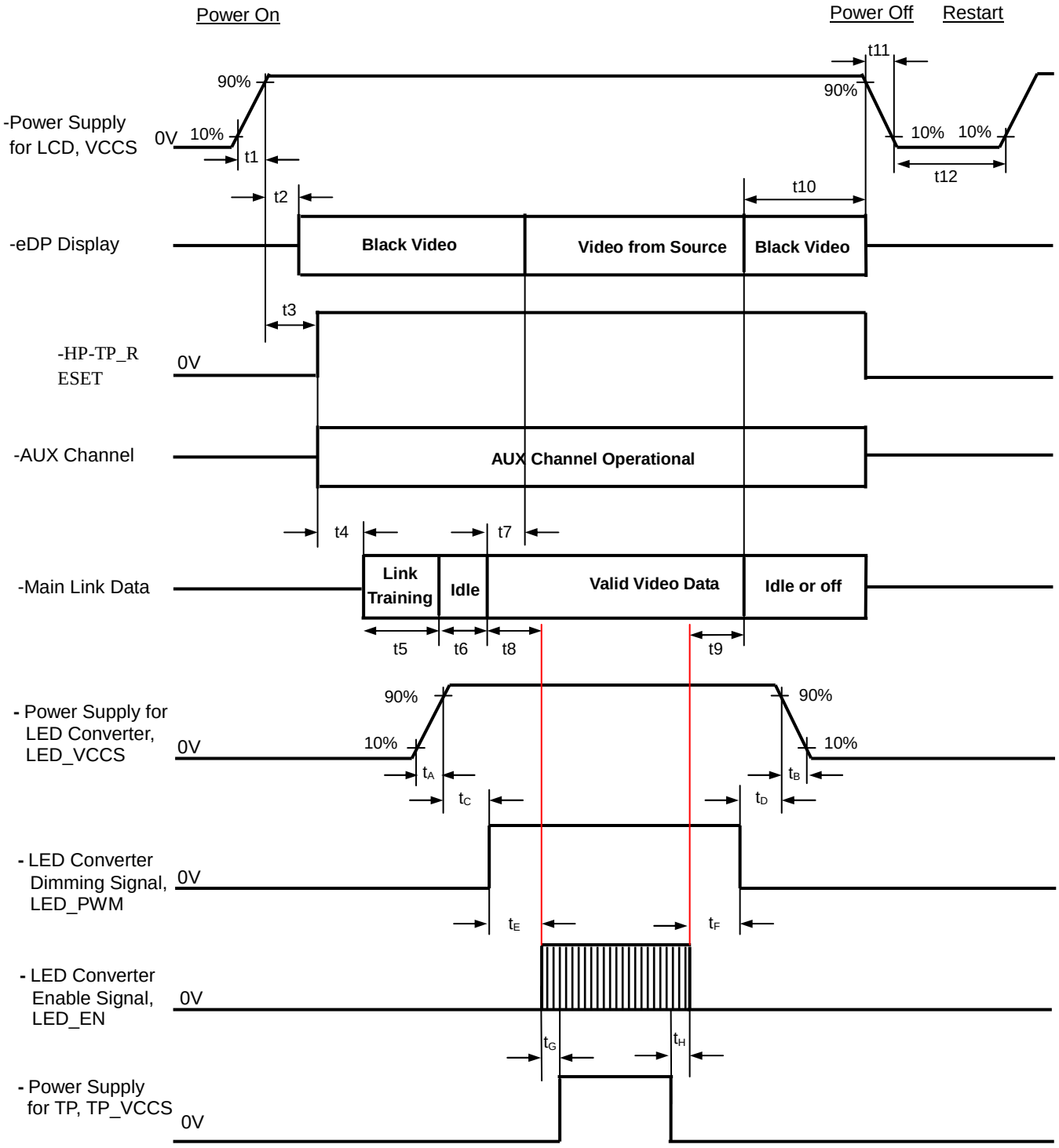
Refresh Rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(72.59)	(76.42)	(80.24)	MHz	-
DE	Vertical Total Time	TV	(790)	(800)	(830)	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	(32)	TV-TVD	TH	-
	Horizontal Total Time	TH	(1566)	(1592)	(1716)	Tc	-
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	-
	Horizontal Active Blanking Period	THB	TH-THB	(226)	TH-THB	Tc	-

INPUT SIGNAL TIMING DIAGRAM



7.5 POWER ON/OFF SEQUENCE



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-

t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	(0)	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	(0)	-	ms	-
t_G	Delay from LED enable signal to TP_VCCS	Source	0		ms	Note(5)
t_H	Delay from TP_VCCS to LED enable signal	Source	0		ms	Note(5)

Note (1) Please don't plug or unplug the interface cable when system is turned on. Before LCD_VCCS and LED_VCCS are ready, it is recommended to pull down the backlight control signals

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

Note (5) Please refer to section 8.3 TOUCH POWER ON/OFF SEQUENCE to obtain detailed timing.

8. TP MODULE ELECTRICAL CHARACTERISTICS

8.1 TP MODULE ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Voltage from TP_VCCS to AGND and DGND	TP_VCCS	-	5.5	V	
Logic Input Voltage		-	3.6	V	

8.2 TP MODULE ELECTRICAL CHARACTERISTICS

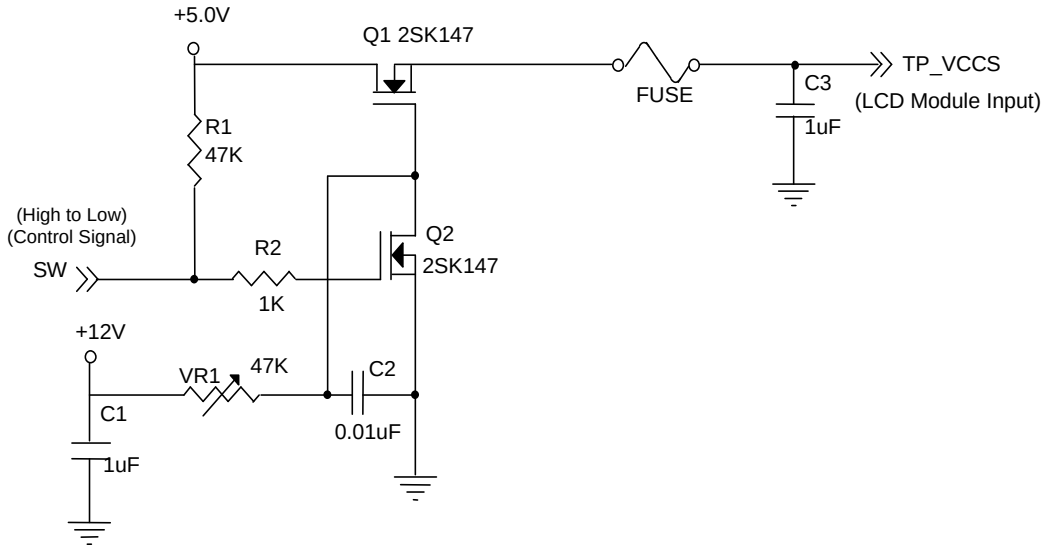
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		TP_VCCS	(4.5)	5.0	(5.5)	V	(1)
Ripple Voltage		TP_V_{RP}			100	mV	(1)
Inrush Current		TP_I_{RUSH}	-	-	(1.8)	A	(1),(2)
Power Supply Current	Active Mode	TP_I_{CC}		(62.5)	(65)	mA	
	Idle Mode			(32)	(35)	mA	
TP_RESET	Normal		1.73	-	3.3	V	(3)
	Active		0	-	1.13	V	(3)
TP_RS	RS High Level		2.31	-	3.3	V	
	RS Low Level		0	-	0.99	V	
USB Signal	D+, D-			3.3		V	(4)

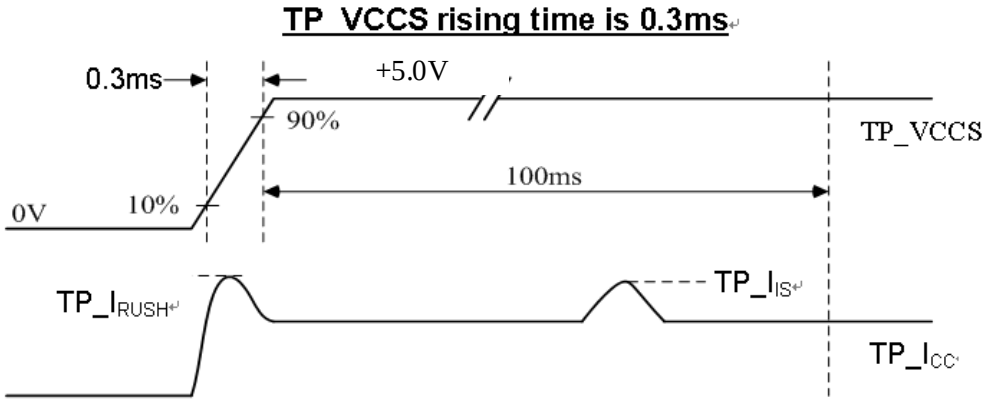
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) TP_I_{RUSH}: the maximum current when TP_VCCS is rising

TP_I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: white



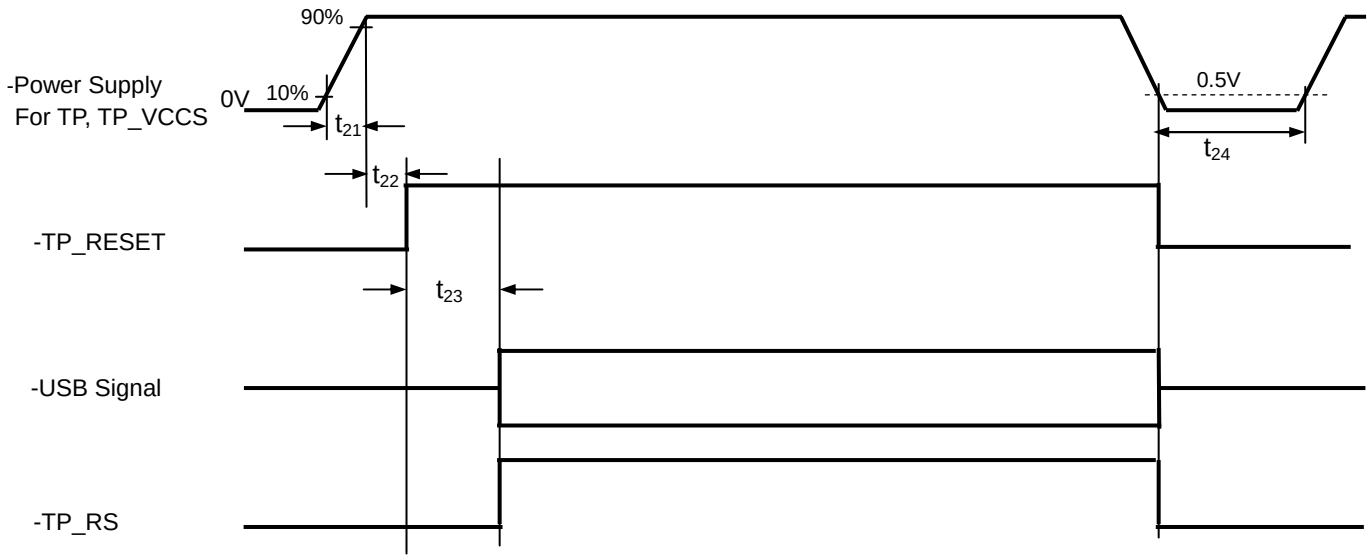


Note (3) TP_RESET is a Schmitt Trigger input. Low to reset Touch IC

Note (4) Follow USB 2.0 standard

Note (5) Please refer to the “windows-pointer-device-protocol, July 24, 2012” regarding the human interface device protocol to communicate with Windows Host.

8.3 TP MODULE POWER ON/OFF SEQUENCE



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t_{21}	TP_VCCS rail rise time, 10% to 90%	Source	0.3	-	ms	-
t_{22}	Delay from TP_VCCS to TP_RESET	Source	0.5	-	ms	-
t_{23}	Delay from TP_RESET to USB signal & TP_RS	Source	25	-	ms	-
t_{24}	TP_VCCS power off duration	Source	10	-	us	-

9. PACKING

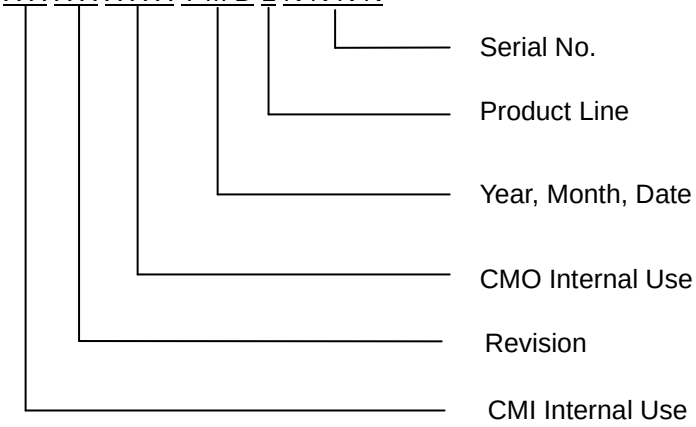
9.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N156BGN - E41

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

9.2 CARTON

(1)Box Dimensions : 490(L)*350(W)*320(H)
(2)20 Module/Carton

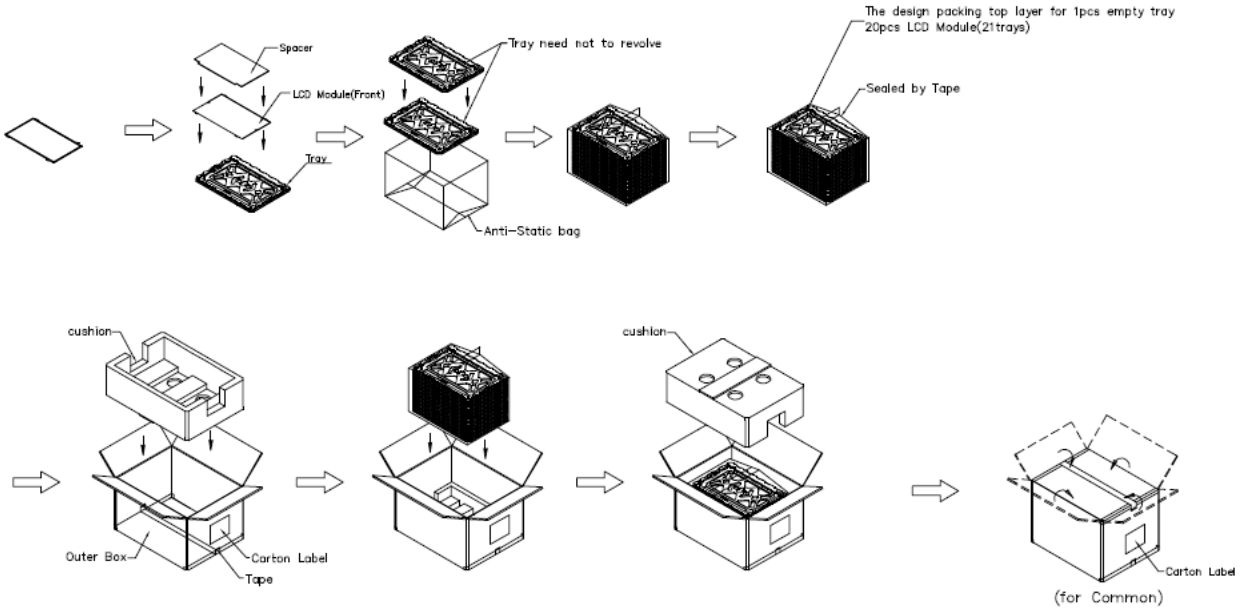


Figure. 9-2 Packing method

9.3 PALLET

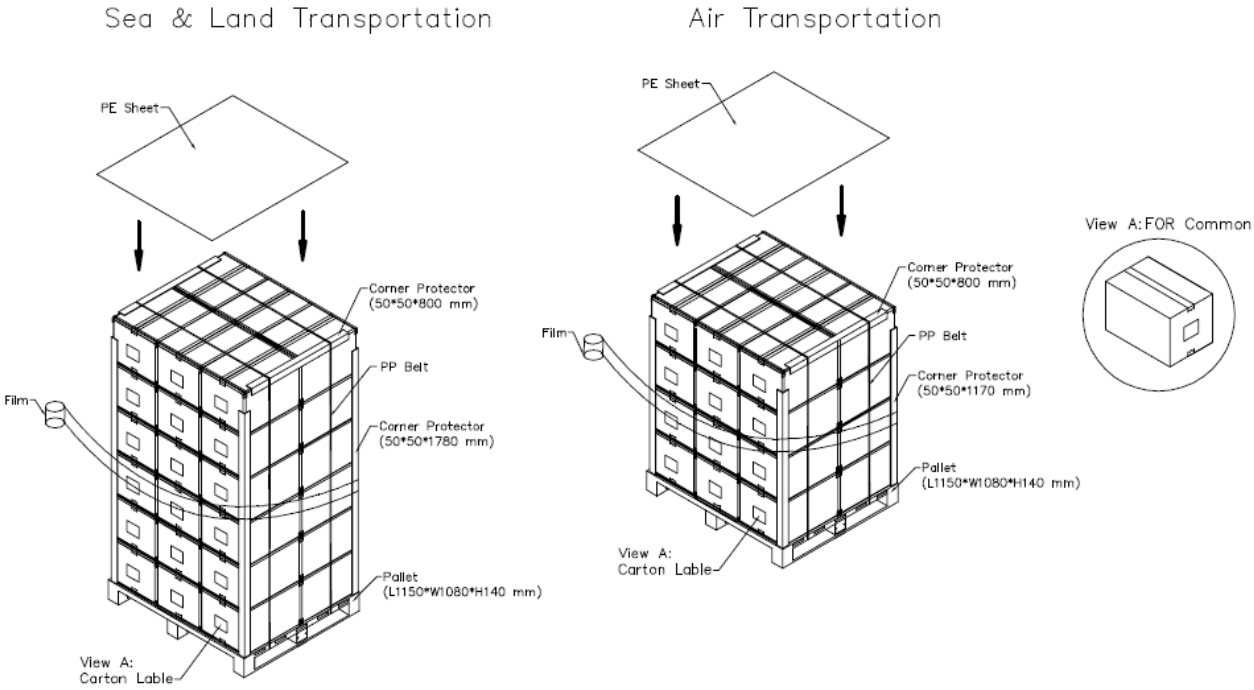


Figure. 9-3 Packing method

10. PRECAUTIONS

10.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

10.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

10.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

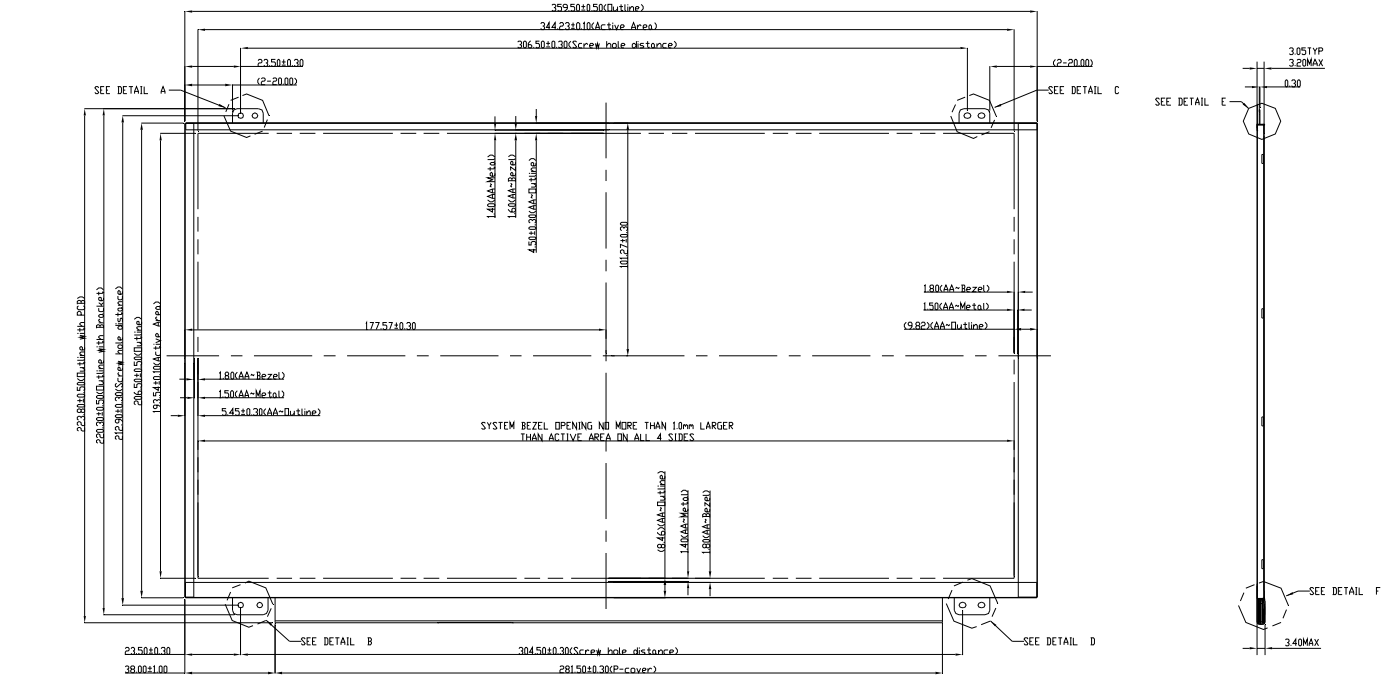
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

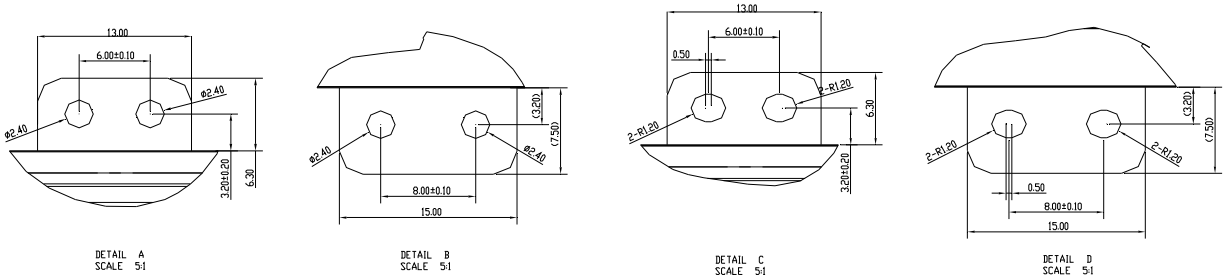
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA ID manufacturer name ("CMN")	0D	00001101
9	09	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	CC	11001100
11	0B	ID product code (MSB)	15	00010101
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	14	00010100
17	11	Year of manufacture (fixed year code)	18	00011000
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("4")	04	00000100
20	14	Video I/P definition ("Digital")	95	10010101
21	15	Active area horizontal (“34.423cm“)	22	00100010
22	16	Active area vertical (“19.354cm“)	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	82	10000010
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	05	00000101
27	1B	Rx=0.572	92	10010010
28	1C	Ry=0.336	56	01010110
29	1D	Gx=0.324	53	01010011
30	1E	Gy=0.584	95	10010101
31	1F	Bx=0.16	29	00101001
32	20	By=0.141	24	00100100
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

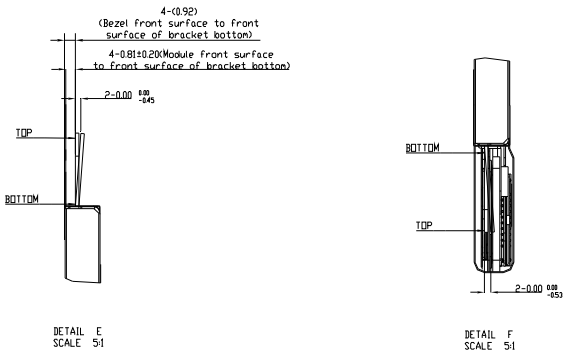
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("76.42MHz")	DA	11011010
55	37	# 1 Pixel clock (hex LSB first)	1D	00011101
56	38	# 1 H active ("1366")	56	01010110
57	39	# 1 H blank ("226")	E2	11100010
58	3A	# 1 H active : H blank	50	01010000
59	3B	# 1 V active ("768")	00	00000000
60	3C	# 1 V blank ("32")	20	00100000
61	3D	# 1 V active : V blank	30	00110000
62	3E	# 1 H sync offset ("68")	44	01000100
63	3F	# 1 H sync pulse width ("45")	2D	00101101
64	40	# 1 V sync offset : V sync pulse width ("4 : 7")	47	01000111
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size (“344 mm“)	58	01011000
67	43	# 1 V image size (“193 mm“)	C1	11000001
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 ASCII string Model name	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name (“N”)	4E	01001110
78	4E	# 2 2nd character of name (“1”)	31	00110001
79	4F	# 2 3rd character of name (“5”)	35	00110101
80	50	# 2 4th character of name (“6”)	36	00110110
81	51	# 2 5th character of name (“B”)	42	01000010
82	52	# 2 6th character of name (“G”)	47	01000111
83	53	# 2 7th character of name (“N”)	4E	01001110
84	54	# 2 8th character of name (“-”)	2D	00101101
85	55	# 2 9th character of name (“E”)	45	01000101
86	56	# 2 10th character of name (“4”)	34	00110100
87	57	# 2 11th character of name (“1”)	31	00110001

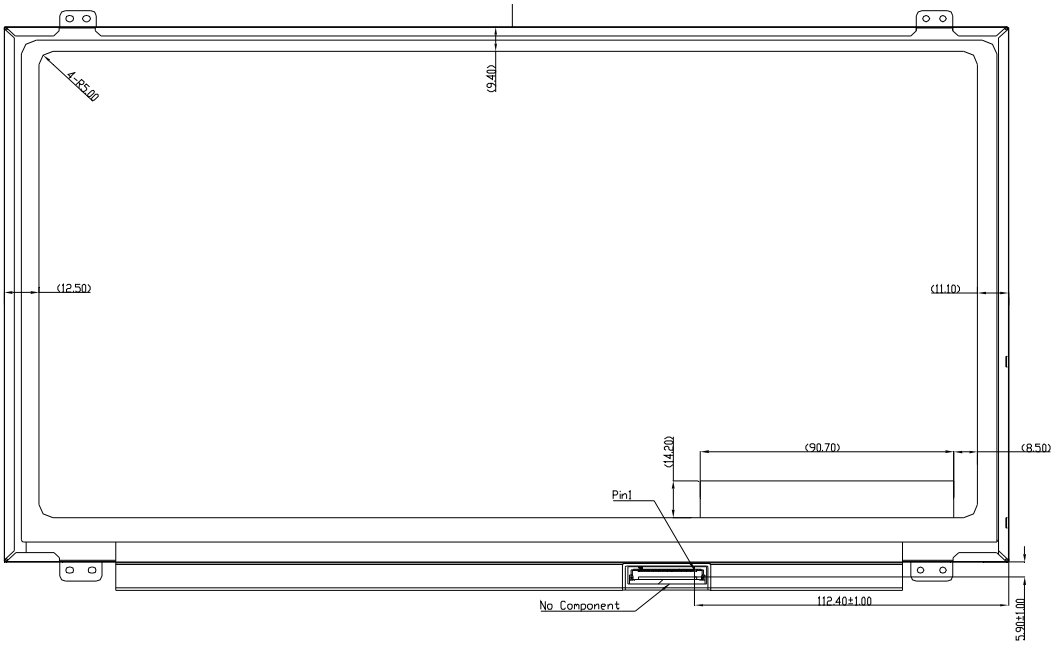
88	58	# 2 New line character indicates end of ASCII string	0A	00001010
89	59	# 2 Padding with “Blank” character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 ASCII string Vendor	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 Character of string ("C")	43	01000011
96	60	# 3 Character of string ("M")	4D	01001101
97	61	# 3 Character of string ("N")	4E	01001110
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 ASCII string Model Name	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name (“N”)	4E	01001110
114	72	# 4 2nd character of name (“1”)	31	00110001
115	73	# 4 3rd character of name (“5”)	35	00110101
116	74	# 4 4th character of name (“6”)	36	00110110
117	75	# 4 5th character of name (“B”)	42	01000010
118	76	# 4 6th character of name (“G”)	47	01000111
119	77	# 4 7th character of name (“N”)	4E	01001110
120	78	# 4 8th character of name (“-”)	2D	00101101
121	79	# 4 9th character of name (“E”)	45	01000101
122	7A	# 4 10th character of name (“4”)	34	00110100
123	7B	# 4 11th character of name (“1”)	31	00110001
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with “Blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	4F	01001111

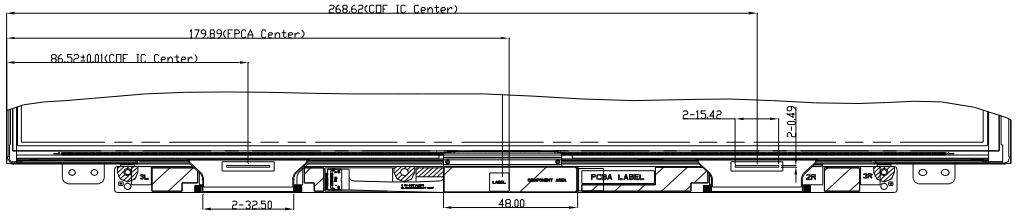
Appendix. OUTLINE DRAWING

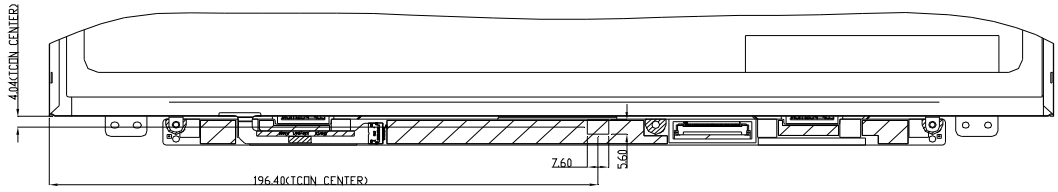








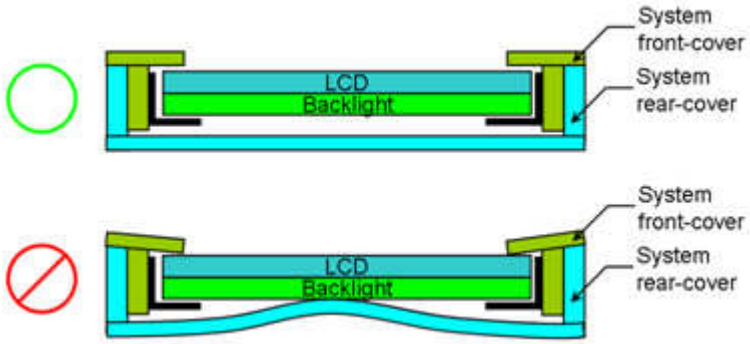
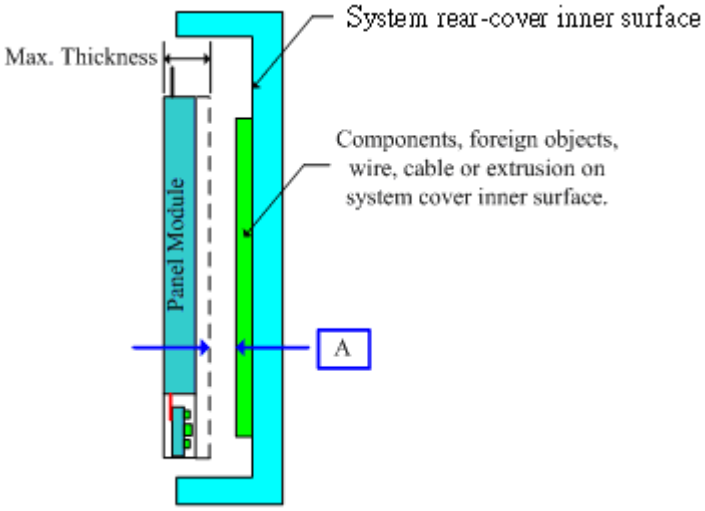


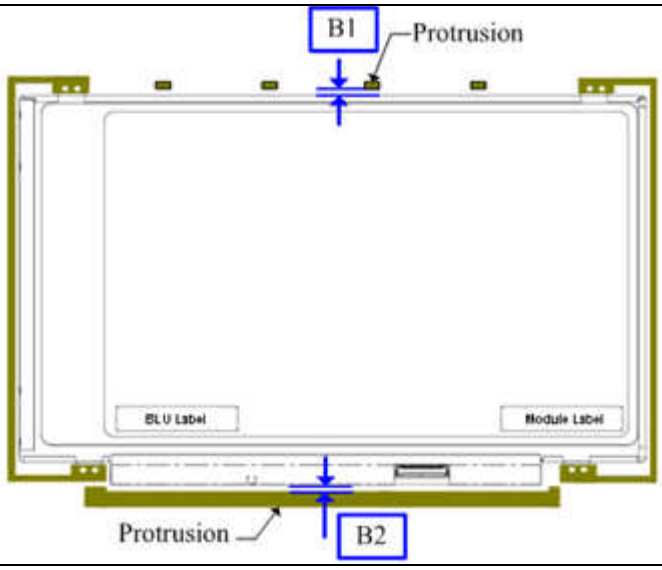


DRIVER IC, COF/FPC, TCON, AND VR LOCATIONS
SEE NOTES FOR EXPLANATION

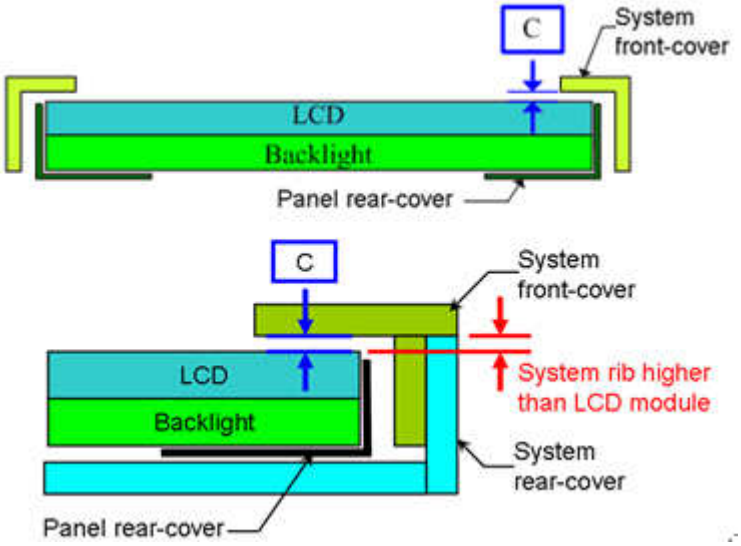
NOTES :
1. LCD MODULE INPUT CONNECTOR : I-PEX 20455-040E-12.
2. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT,
   NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR
   FOREIGN OBJECTS OVER FPC/COF, T-CON AND VR LOCATIONS.
3. LVDS/EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
4. MODULE FLATNESS SPEC 2.00 MM MAX. (SPEC. WILL BE MODIFIED AFTER DVT CHECK).
5. " ( )" MARKS THE REFERENCE DIMENSION.

Appendix. SYSTEM COVER DESIGN GUIDANCE FOR TOD

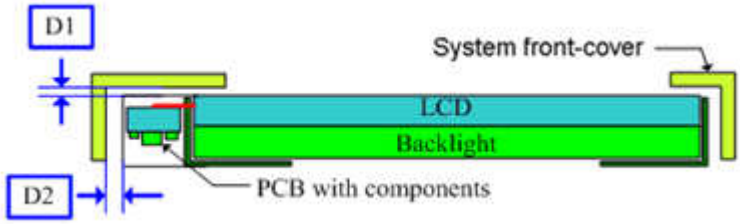
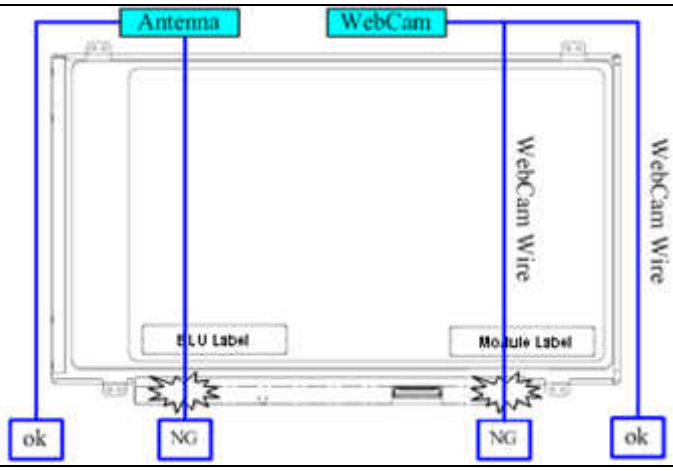
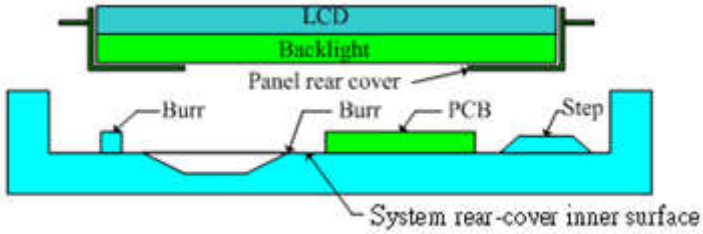
0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Maximum flatness of panel and system rear-cover should be taken into account for gap design. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
2	**Design gap B1 & B2 between panel & protrusions**

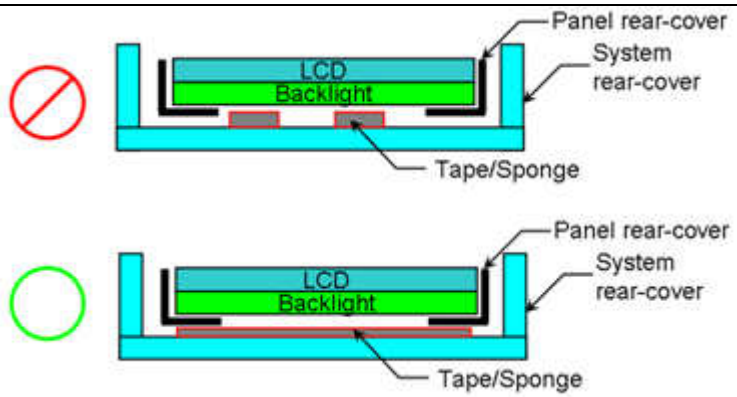


Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Design gap C between system front-cover & panel surface.**

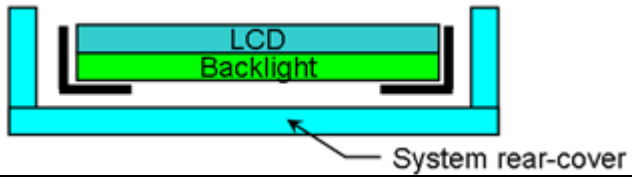


Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
4	**Design gap D1 & D2 between system front-cover & PCB Assembly.**

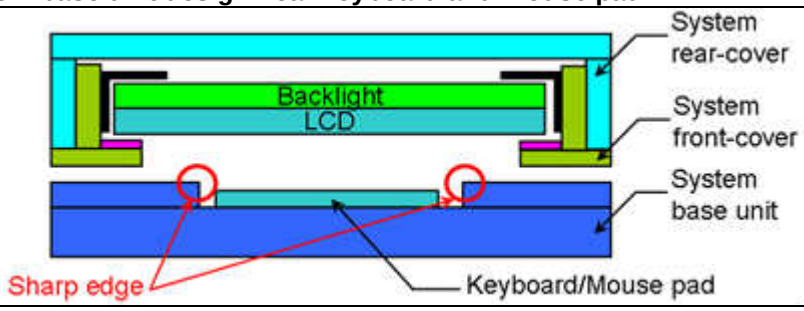
	
Definition	Same as point 2 and 3, but focus on PCBA side.
5	**Interference examination of antenna cable and WebCam wire**
	
Definition	Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
6	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
7	**Tape/sponge design on system inner surface**



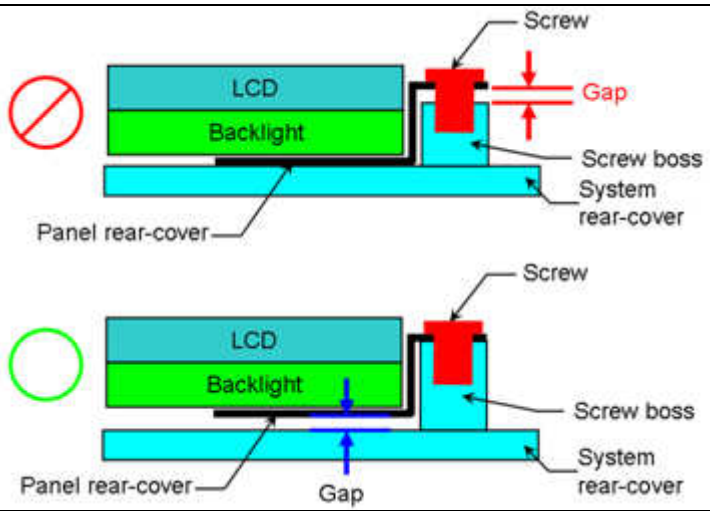
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
8	**Material used for system rear-cover**



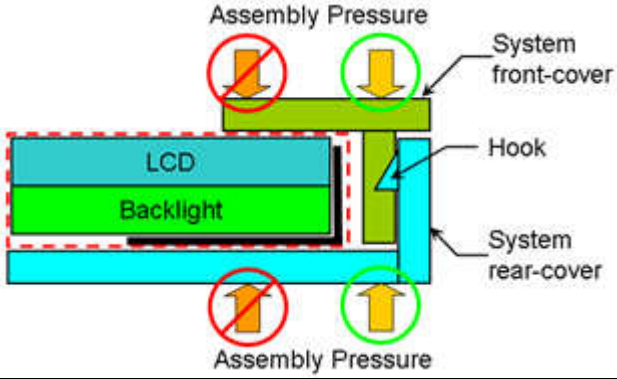
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
9	**System base unit design near keyboard and mouse pad**



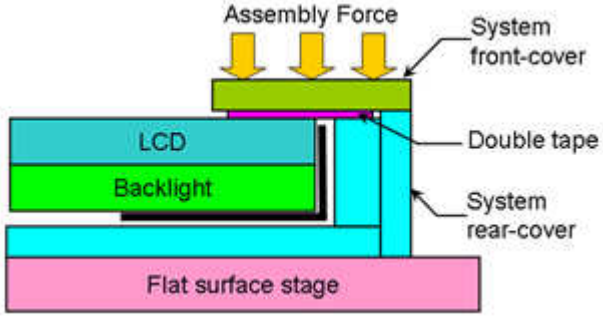
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
10	**Screw boss height design**



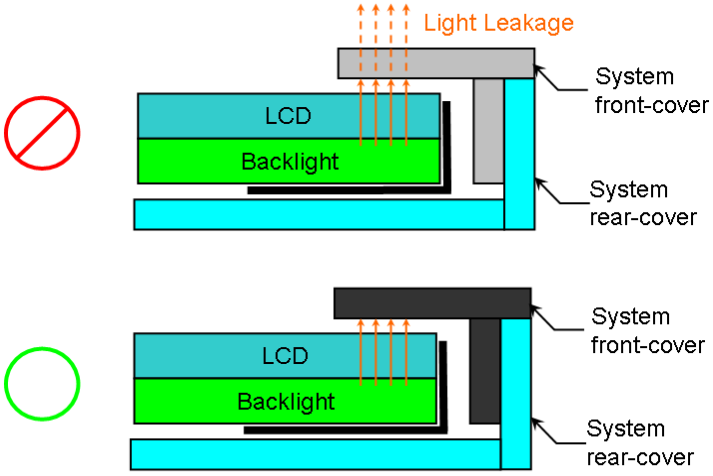
Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
11	**Assembly SOP examination for system front-cover with Hook design**



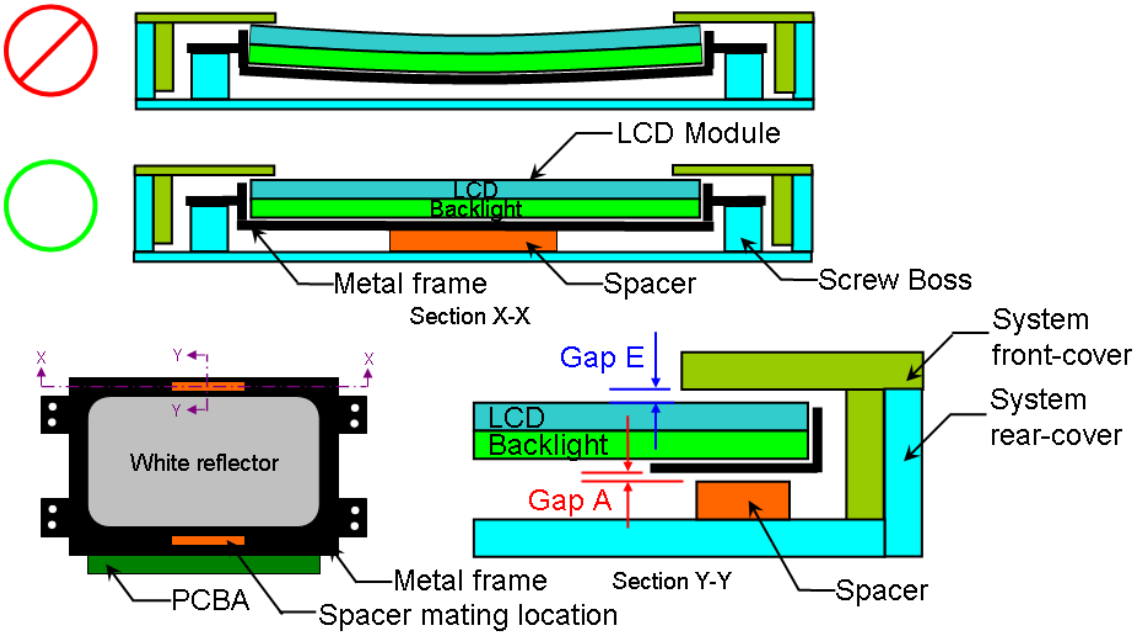
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Assembly SOP examination for system front-cover with Double tape design**



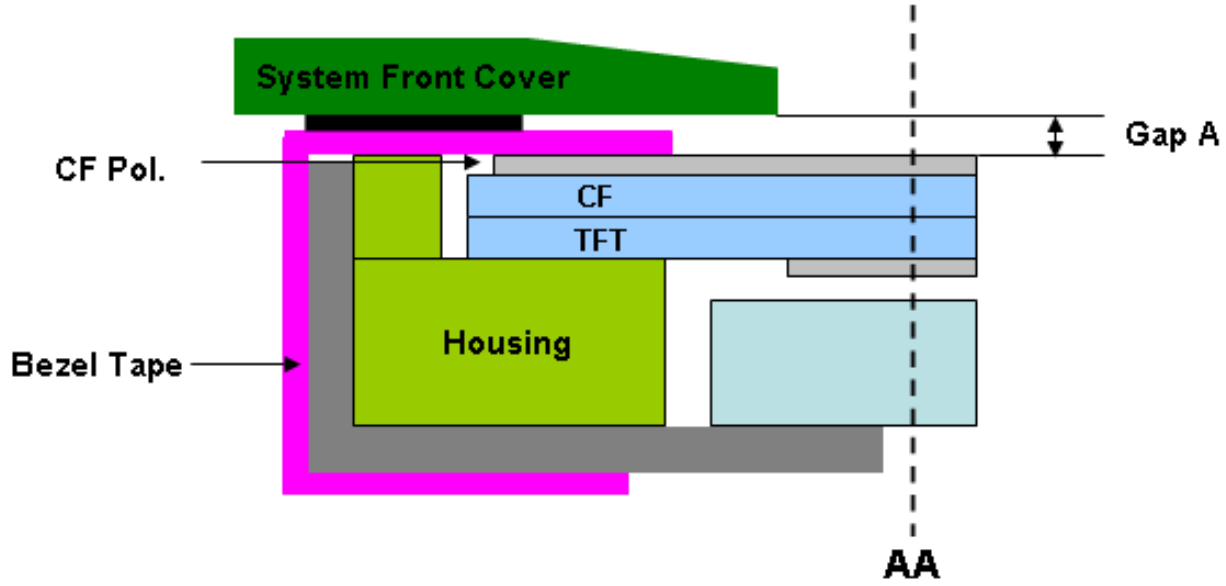
Definition	To prevent panel crack during system front-cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.
13	**Color of system front-cover material**



Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.
14	**Inspection spec of gap E between system front-cover to LCD module surface**

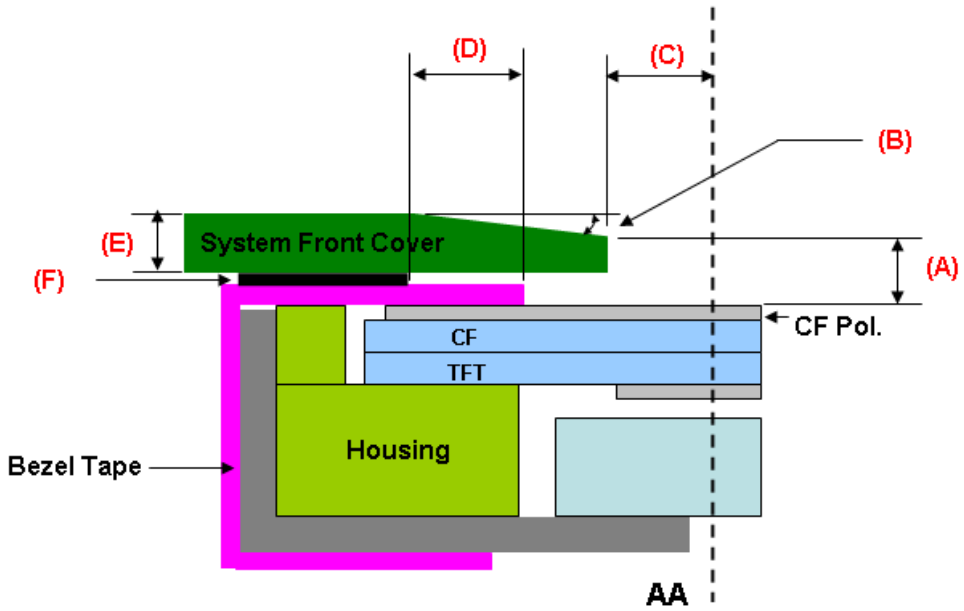


Definition	To maintain gap E (gap of system front-cover to LCD module) in its inspection spec, especially at location with maximum LCD deformation (center of LCD length), we recommend adding spacer with design gap A smaller or equal to gap E. The allowable spacer mating location is on module metal frame outside LCD Active-Area. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
15	**Design Gap between System Front-cover & TOD LCD module surface**



0.15≦ Gap A ≦ 0.20 mm

Definition	Gap A between system front-cover & TOD LCD module surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap for first graph, design value for front-cover depth is recommended higher than module wing depth.
16	**System Front-cover dimension suggestion**

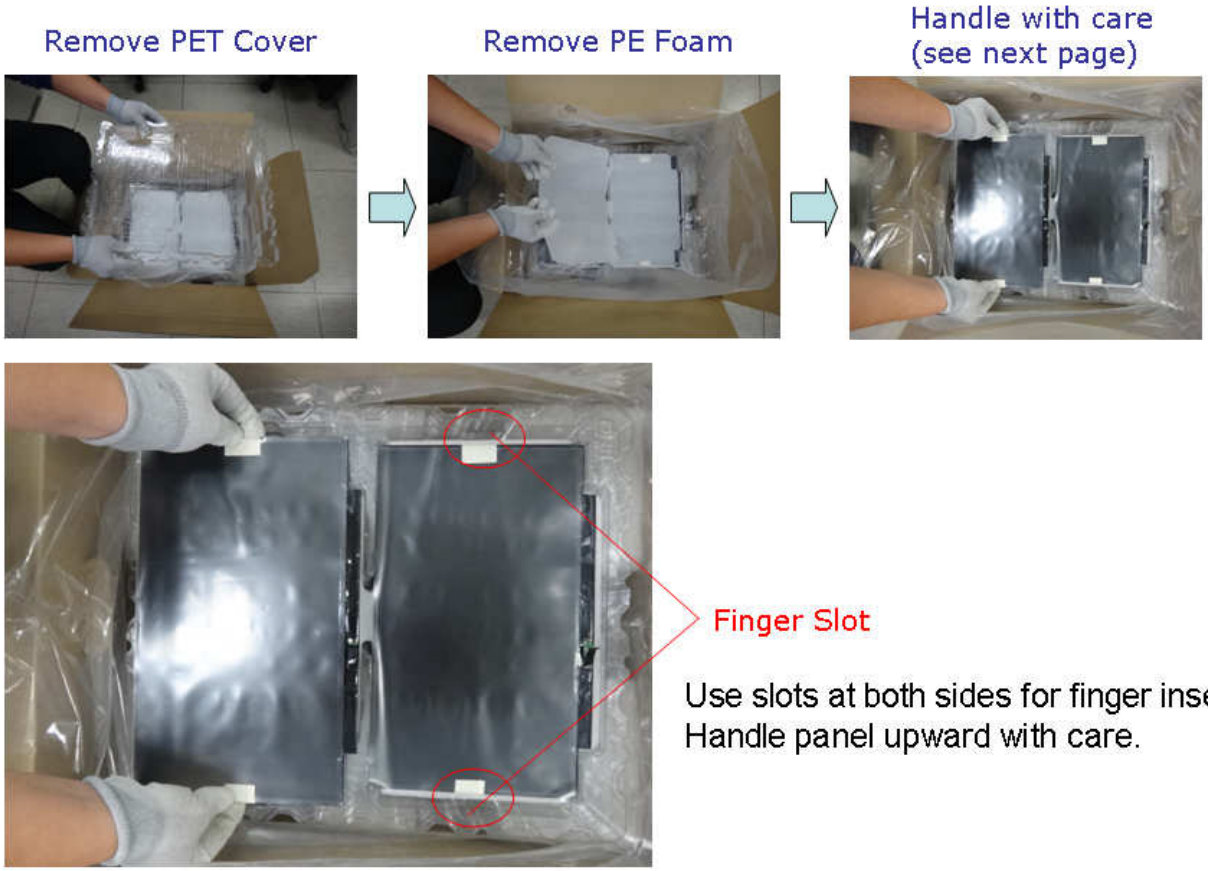


System Front Cover Open TOP to CF Pol. (A)	System Front Cover Chamfer (B)	System Front Cover Open to AA (C)	Bezel Tape Edge to Double Tape (D)	System Front Cover thickness (E)	Double Tape Thickness (F)
0.8mm Max	8~20°	0.7≦ (B) ≦ 0.9mm	1.0 mm Min	1.2mm MAX	0.05≦ (F) ≦ 0.08mm

CAUTION : In order to avoid the risk of bezel tape peeling, INX suggest not to attach any double tape on bezel tape; if necessary, the location of duuble tape attach must follow INX design guidance.	
Definition	To achieve better touch sensibility, INX suggests to follow design value as recommended , Recommended dimension is shown in above graph.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**
	
2.	**Panel Lifting**



3.	**Do and Don't**

Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

- Lifting with one hand.

- Handle at PCBA side.

Don't :

- Stack panels.

- Press panel.

Don't :

- Put foreign stuff onto panel

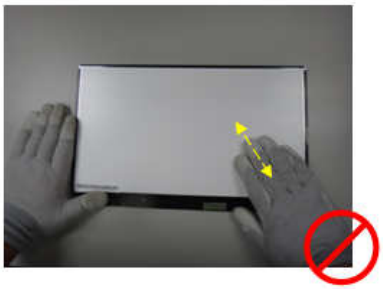
- Put foreign stuff under panel

Don't :

- Paste any material unto white reflector sheet

Don't :

- Pull / Push white reflector sheet



Don't :

- Hold at panel corner.

Don't :

- Twist panel.

Do :

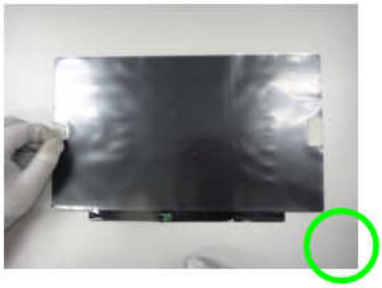
- Hold panel at top edge while inserting connector.

Don't :

- Press white reflector sheet while inserting connector.

Do :

- Remove panel protector film starts from side tape.



Don't :

- Remove panel protector film from film corner directly before side tape is removed.

Don't :

- Touch or Press PCBA Area.